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| 10/750,843 | 01/05/2004 | Howard E. Rhodes | M4065.0947/P947 | 2490 |

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| EXAMINER | |
|---|---|
| MONDT, JOHANNES P | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

DATE MAILED: 08/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/750,843 | RHODES, HOWARD E. | |
| | Examiner | Art Unit | |
| | Johannes P. Mondt | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-64* is/are pending in the application.

4a) Of the above claim(s) *39-64* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/28/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

Applicant's election without traverse of the Group I invention (claims 1-38) in the reply filed on 6/14/05 is acknowledged.

### *Information Disclosure Statement*

The examiner has considered the item listed on the Information Disclosure Statement filed 6/28/2004. A signed copy of Substitute Form PTO-1449 is herewith enclosed.

### *Drawings*

1. ***Figures 1-3*** should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

2. ***Claim 9*** is objected to because of the following informalities: the wordings in "(5T)" (line 2), "(6T)" (line 2) and "(7T)" should be removed. Appropriate correction is required.

3. ***Claim 10*** is objected to because of the following informalities: the wording "(HDR)" (line 4) should be removed. Appropriate correction is required.

4. ***Claim 11*** objected to because of the following informalities: the wording "($V_{dd}$)" (line 3) should be removed. Appropriate correction is required.

5. ***Claim 13*** is objected to because of the following informalities: the wording "(4T)" (line 2) should be removed. Appropriate correction is required.

6. ***Claim 14*** is objected to because of the following informalities: the wording "(6T)" (line 2) should be removed. Appropriate correction is required.

7. ***Claim 15*** is objected to because of the following informalities: the wording "(7T)" (line 2) should be removed. Appropriate correction is required.

8. ***Claim 29*** is objected to because of the following informalities: the wordings "(4T)" (line 2), "(5T)" (line 2), "(6T)" (line 2) and "(7T)" (line 3) should be removed. Appropriate correction is required.

9. ***Claim 30*** is objected to because of the following informalities: the wording "(HDR)" (line 4) should be removed. Appropriate correction is required.

10. ***Claim 31*** is objected to because of the following informalities: the wording "($V_{dd}$)" (line 3) should be removed. Appropriate correction is required.

11. ***Claim 32*** is objected to because of the following informalities: the wording "$V_{dd}$" (line 3) should be removed. Appropriate correction is required.

12. ***Claim 34*** is objected to because of the following informalities: the wording "(6T)" (line 2) should be removed. Appropriate correction is required.

13. ***Claim 35*** is objected to because of the following informalities: the wording "(7T)" (line 2) should be removed. Appropriate correction is required.

### *Specification*

The following is a quotation from the relevant sections of the Patent Rules under 37 C.F.R. 1.75 that form the basis of the objection made in this office action.

(d)

(1) The claim or claims must conform to the invention as set forth in the remainder of the specification and the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description (see § 1.58(a)).

The Specification is objected to because the remainder of the Specification, i.e., other than the claims, does not disclose seven-transistor pixels as recited in claims 9, 29 and 35. The Specification should be amended to include said disclosure without, however, introducing any new matter. Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

15. ***Claims 1-14 and 16-18*** are rejected under 35 U.S.C. 102(b) as being anticipated by Pain et al (6,326,230 B1). Pain et al teach a method of operating a pixel cell of an imager (title, abstract, col. 2, l. 64 – col. 3, l. 8 and claims 1-11 In Pain et al), the method comprising:

accumulating charge at a photo-conversion device (either photo-gate 52 of transistor PG: Figure 2A and col. 4, l. 39-43, or a photodiode 120: Figure 5A) during an integration period (see claim 8 in Pain et al);

storing accumulated charge from said photo-conversion device 52 or 120 at a charge collection region 54 or 154, respectively (Figures 2A and 5A; col. 4, l. 39-54 and col. 7, l. 15-16 and 56-63) (claim 8 in Pain et al: said charge collection region is the sense node);

reading out (through transistors $M_{sel}$ and $M_{in}$ (col. 4, l. 58-66 and col. 7, l. 25-37) said charge from said charge collection region (see claim 9 in Pain et al); and

removing residual charge remaining in said photo-conversion device prior to a subsequent integration period (through signals to TX, TX2 and RST transistors) (col. 6, l. 33-40 and col. 8, l. 50-65) (see claim 11 in Pain et al).

*On claim 2:* said act of removing comprises activating at least one of a reset transistor and a transfer transistor (see claim 11) to couple said photo-conversion device to a potential prior to said subsequent integration period (cf. Fig. 6D: and col. 6, l. 34-37).

*On claim 3:* said reset transistor and said transfer transistor are activated substantially simultaneously (see Fig. 6D, traces TX2 and RST or traces TX and RST (transfer (TX and TX2) and reset (RST) transistors, respectively.; see col. 7, l. 47 – col. 8, l. 6).

*On claim 4:* said substantially simultaneous activation of said reset transistor RST and said transfer transistor TX occurs after said act of reading out said charge (col. 9, l. 1-4).

*On claim 5:* said act of transferring by transfer gate TX comprises transferring charge from said photoconversion device (from 120) (col. 7, l. 5-11) to a floating diffusion region (to 154) (col. 7, l. 25-28).

*On claim 6:* said act of storing charge comprises transferring said charge to said floating diffusion region 154 via said transfer transistor TX (col. 7, l. 25-37).

*On claim 7:* said act of transferring comprises transferring charge from said photo-conversion device 120 to a supply voltage Vdd (through transfer transistor TX2 (col. 7, l. 23-25).

*On claim 8:* said act of reading out comprises reading out said charge with a transistor $M_{in}$ (col. 7, l. 25-37).

*On claim 9:* the pixel cell is at least one of a five transistor (5T) pixel, a six transistor pixel (6T) or a seven transistor pixel (7T), as witnessed by transistors TX, TX2, RST already discussed, and source-follower transistor $M_{in}$ (col. 7, l. 25-37) and pixel selection switch transistor $M_{sel}$ (col. 7, l. 25-37).

*On claim 10:* the act of removing comprises activating a transistor electrically connected to said photo-conversion device wherein said transistor includes at least one of a global shutter, anti-blooming device or high dynamic range transistor (HDR), namely an anti-blooming device through appropriate selection of the voltage on the gate of transfer transistor TX2 (col. 8, l. 40-42).

*On claim 11:* the act of activating said transistor TX2 allows residual charge to move from said photo-conversion device 120 to a supply voltage ($V_{dd}$) (at power supply node 164: see col. 7, l. 22-25).

*On claim 12:* the imager is a CMOS imager (col. 3, l. 38-55 and col. 4, l. 23-38).

*On claim 13:* the CMOS imager comprises four transistor (4T) pixels (TX, TX2, RST, and $M_{in}$). (loc.cit.).

*On claim 14:* the CMOS imager with photo-gate 54 (embodiment of Figures 2A) comprises six transistor (6T) pixels (namely: TX, TX2, RST, $M_{in}$, ROW ($M_{sel}$), and PG (col. 4, l. 39-43)).

*On claim 16:* said photo-conversion device 120 is a photodiode (col. 7, l. 5-21).

*On claim 17:* said photo-conversion device 52 is a photo-gate (col. 4, l. 39-47).

*On claim 18:* said photo-conversion device 52, being a photo-gate, inherently is a photoconductor, because conduction charges are produced by impinging but neutral light, whereby the conductivity of the photo-gate is changed.

### ***Claim Rejections - 35 USC § 103***

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. ***Claims 15 and 19-38*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Pain et al (6,326,230 B1) in view of Rhodes (6,140,630).

*On claims 15 and 35:* Although Pain et al six transistor (6T) pixels (see claims 14 and 34 (for claim 34 see below) in this application) they do not necessarily teach the further limitation defined by claim 15 or claim 35. However, it would have been obvious to include said further limitation in view of Rhodes, who, in a patent incorporated by reference in Applicant's application of its relevance and hence analogous art, teach the inclusion of a load transistor 39 so as to provide an option to either load and collect the read charge through the sample and hold circuit or ground the sample. *Motivation* to include the teaching by Rhodes derives from the creation of said option.

*On claim 19:* Pain et al teach a method for operating a pixel cell of an imager (title, abstract, col. 2, l. 64 – col. 3, l. 8 and claims 1-11 In Pain et al), the method comprising:

resetting a charge collection region (54 or 154) with a reset transistor RST during a reset period (see: col. 6, l. 33-40 and col. 8, l. 50-65 and claim 11 in Pain et al);

accumulating charge at a photo-conversion device 52 or 120 during an integration period (either photo-gate 52 of transistor PG: Figure 2A and col. 4, l. 39-43, or a photodiode 120: Figure 5A; and see claim 8 in Pain et al);

storing accumulated charge from said photo-conversion device at said charge collection region via a transfer transistor TX (Figures 2A and 5A; col. 4, l. 39-54 and col. 7, l. 15-16 and 56-63) (claim 8 in Pain et al: said charge collection region is the sense node);

reading out said charge from said charge collection region (through transistors $M_{sel}$ and $M_{in}$ (col. 4, l. 58-66 and col. 7, l. 25-37); and

removing residual charge remaining in said photo-conversion device after said charge storage at said charge collection region (through signals to TX, TX2 and RST transistors) (col. 6, l. 33-40 and col. 8, l. 50-65) (see claim 11 in Pain et al),

wherein said act of removing comprises activating said reset transistor and said transfer transistor prior to a subsequent integration period (cf. Fig. 6D: and col. 6, l. 34-40).

*Pain et al do not necessarily teach* the limitation that said reading out is being conducted not merely to a sample circuit but to a sample and hold circuit. However, it would have been obvious to include said limitation in view of Rhodes who teaches said reading out to be conducted to a sample and hold circuit (S/H circuit within read circuit 60 in Figure 1: see col. 3, l. 57 – col. 4, l. 37) thus enabling comparisons of signals from different pixels by which pixels variations can be eliminated (col. 25-36).

*Motivation to* include the teaching by Rhodes is the ability to hold the signal after sampling with further processing steps such as signal subtraction to eliminate pixel variations.

. *On claim 20:* said act of removing comprises activating said reset transistor and said transfer transistor substantially simultaneously (see Fig. 6D, traces TX2 and RST or traces TX and RST (transfer (TX and TX2) and reset (RST) transistors, respectively.; see col. 7, l. 47 – col. 8, l. 6).

*On claim 21:* said substantially simultaneous activation of said reset transistor RST and said transfer transistor TX occurs after said act of reading out said charge (col. 9, l. 1-4).

*On claim 22:* said act of transferring comprises transferring charge (through transfer transistor TX2) from said photo-conversion device (either 52 or 120) to a supply voltage Vdd (col. 4, l. 49-54) and col. 7, l. 23-25).

*On claim 23:* the imager is a CMOS imager (col. 3, l. 38-55 and col. 4, l. 23-38).

*On claim 24:*the CMOS imager comprises a four-transistor, five-transistor, six transistor or seven transistor pixel architecture, as witnessed by transistors TX, TX2, RST already discussed, and source-follower transistor $M_{in}$ (col. 7, l. 25-37) and pixel selection switch transistor $M_{sel}$ (col. 7, l. 25-37).

*On claim 25:* said photo-conversion device 120 is a photodiode (col. 7, l. 5-21).

*On claim 26:* said photo-conversion device 52 is a photo-gate (col. 4, l. 39-47).

*On claim 27:* said photo-conversion device 52, being a photo-gate, inherently is a photoconductor, because conduction charges are produced by impinging but neutral light, whereby the conductivity of the photo-gate is changed.

*On claim 28:* A method for operating a pixel cell of an imager (title, abstract, col. 2, l. 64 – col. 3, l. 8 and claims 1-11 In Pain et al), the method comprising:

resetting a charge collection region 54 or 154 (loc.cit.) with a reset transistor during a reset period (see: col. 6, l. 33-40 and col. 8, l. 50-65 and claim 11 in Pain et al);

accumulating charge at a photo-conversion device during an integration

period (either photo-gate 52 of transistor PG: Figure 2A and col. 4, l. 39-43, or a photodiode 120: Figure 5A; and see claim 8 in Pain et al);

storing accumulated charge from said photo-conversion device at said charge collection region via a transfer transistor TX (Figures 2A and 5A; col. 4, l. 39-54 and col. 7, l. 15-16 and 56-63) (claim 8 in Pain et al: said charge collection region is the sense node);

reading out said charge from said charge collection region (through transistors $M_{sel}$ and $M_{in}$ (col. 4, l. 58-66 and col. 7, l. 25-37); and

removing residual charge remaining in said photo-conversion device after said charge storage at said charge collection region (through signals to TX, TX2 and RST transistors) (col. 6, l. 33-40 and col. 8, l. 50-65) (see claim 11 in Pain et al),

wherein said act of removing comprises activating a transistor TX2 electrically connected to said photo-conversion device 120 prior to a subsequent integration period (the transfer transistor TX2 is electrically connected to the photodiode because said photodiode forms a source/drain region of said transistor TX2) (cf. Figure 5A and loc.cit.).

*Pain et al do not necessarily teach* the limitation that said reading out is being conducted not merely to a sample circuit but to a sample and hold circuit. However, it would have been obvious to include said limitation in view of Rhodes who teaches said reading out to be conducted to a sample and hold circuit (S/H circuit within read circuit 60 in Figure 1: see col. 3, l. 57 – col. 4, l. 37) thus enabling comparisons of signals from different pixels by which pixels variations can be eliminated (col. 25-36).

*Motivation to* include the teaching by Rhodes is the ability to hold the signal after sampling with further processing steps such as signal subtraction to eliminate pixel variations.

*On claim 29:* the CMOS imager comprises a four-transistor, five-transistor, six transistor or seven transistor pixel architecture, as witnessed by transistors TX, TX2, RST already discussed, and source-follower transistor $M_{in}$ (col. 7, l. 25-37) and pixel selection switch transistor $M_{sel}$ (col. 7, l. 25-37).

*On claim 30:* the act of removing comprises activating a transistor electrically connected to said photo-conversion device wherein said transistor includes at least one of a global shutter, anti-blooming device or high dynamic range transistor (HDR), namely an anti-blooming device through appropriate selection of the voltage on the gate of transfer transistor TX2 (col. 8, l. 40-42).

*On claim 31:* the act of activating said transistor TX2 allows residual charge to move from said photo-conversion device 120 to a supply voltage ($V_{dd}$) (at power supply node 164: see col. 7, l. 22-25).

*On claim 32:* said act of transferring comprises transferring charge from said photo-conversion device to a supply voltage ($V_{dd}$) (at node 64 or node 164: see col. 4, l. 55-57 and col. 7, l. 22-25)

*On claim 33:* the imager is a CMOS imager (col. 3, l. 38-55 and col. 4, l. 23-38).

*On claim 34:* the CMOS imager with photo-gate 54 (embodiment of Figures 2A) comprises six transistor (6T) pixels (namely: TX, TX2, RST, $M_{in}$, ROW ($M_{sel}$), and PG (col. 4, l. 39-43)).

*On claim 36:* said photo-conversion device 120 is a photodiode (col. 7, l. 5-21).

*On claim 37:* said photo-conversion device 52 is a photo-gate (col. 4, l. 39-47).

*On claim 38:* said photo-conversion device 52, being a photo-gate, inherently is a photoconductor, because conduction charges are produced by impinging but neutral light, whereby the conductivity of the photo-gate is changed.

***Conclusion***

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Mann et al (US 2002/0190287 A1); and Chi (6,064,053), the latter made of record by Applicant in IDS of 6/28/04.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
July 31, 2005

Patent Examiner:

Johannes Mondt (Art Unit: 2826).

EVAN PERT
PRIMARY EXAMINER